



1Mb x 36, 2Mb x 18
36Mb SYNCHRONOUS PIPELINED,
SINGLE CYCLE DESELECT STATIC RAM

JUNE 2010

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- Power Supply
LPS: $V_{DD} 3.3V \pm 5\%$, $V_{DDQ} 3.3V/2.5V \pm 5\%$
VPS: $V_{DD} 2.5V \pm 5\%$, $V_{DDQ} 2.5V \pm 5\%$
- JEDEC 100-Pin TQFP and 165-ball PBGA packages
- Lead-free available

DESCRIPTION

The *ISSI* IS61LPS/VPS102436A and IS61LPS/VPS204818A are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPS/VPS102436A is organized as 1,048,476 words by 36 bits. The IS61LPS/VPS204818A is organized as 2M-word by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable (\overline{BWE}) input combined with one or more individual byte write signals (\overline{BWx}). In addition, Global Write (\overline{GW}) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either \overline{ADSP} (Address Status Processor) or \overline{ADSC} (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the \overline{ADV} (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

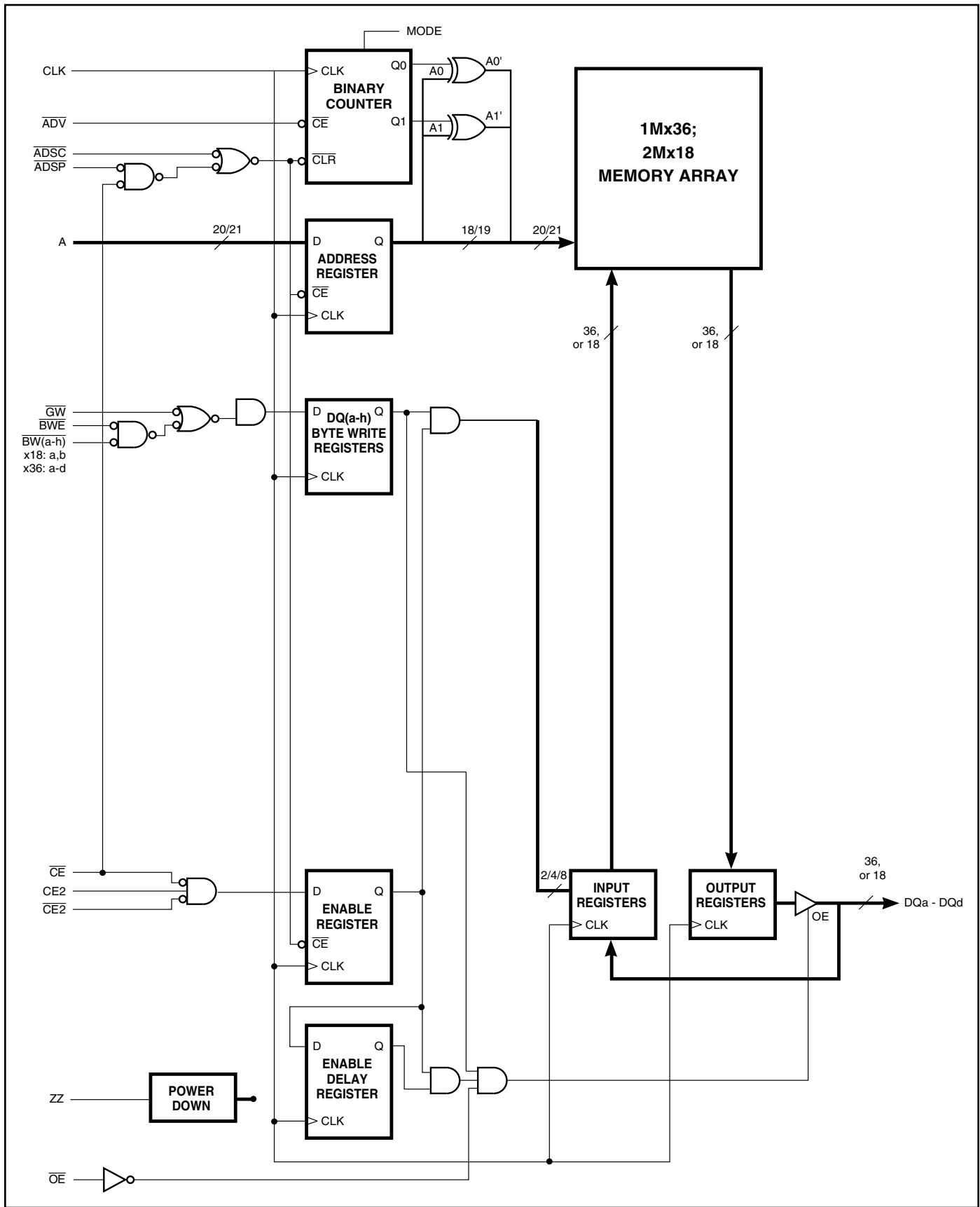
| Symbol | Parameter | 200 | 166 | Units |
|--------|-------------------|-----|-----|-------|
| tkQ | Clock Access Time | 3.1 | 3.5 | ns |
| tkC | Cycle Time | 5 | 6 | ns |
| | Frequency | 200 | 166 | MHz |

Copyright © 2010 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

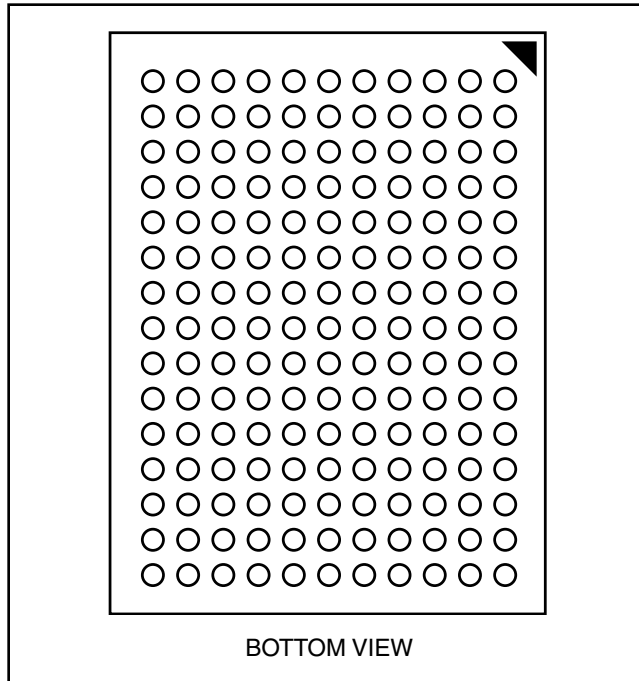
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

BLOCK DIAGRAM



165-PIN BGA

165-Ball, 13x15 mm BGA
1mm Ball Pitch, 11x15 Ball Array



165 PBGA PACKAGE PIN CONFIGURATION

1M x 36 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|----------|------|-----|-----------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-----|------|
| A | NC | A | \overline{CE} | \overline{BWc} | \overline{BWb} | $\overline{CE2}$ | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A | NC |
| B | NC | A | CE2 | \overline{BWd} | \overline{BWa} | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A | NC |
| C | DQPc | NC | VDDQ | Vss | Vss | Vss | Vss | Vss | VDDQ | NC | DQPb |
| D | DQc | DQc | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQb | DQb |
| E | DQc | DQc | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQb | DQb |
| F | DQc | DQc | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQb | DQb |
| G | DQc | DQc | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQb | DQb |
| H | NC | NC | NC | VDD | Vss | Vss | Vss | VDD | NC | NC | ZZ |
| J | DQd | DQd | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQa | DQa |
| K | DQd | DQd | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQa | DQa |
| L | DQd | DQd | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQa | DQa |
| M | DQd | DQd | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQa | DQa |
| N | DQPd | NC | VDDQ | Vss | NC | A | NC | Vss | VDDQ | NC | DQPd |
| P | NC | NC | A | A | NC | A1* | NC | A | A | A | A |
| R | MODE | A | A | A | NC | A0* | NC | A | A | A | A |

Note: * A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|--|-----------------------------------|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| \overline{ADV} | Synchronous Burst Address Advance |
| \overline{ADSP} | Address Status Processor |
| \overline{ADSC} | Address Status Controller |
| \overline{GW} | Global Write Enable |
| CLK | Synchronous Clock |
| \overline{CE} , $\overline{CE2}$, CE2 | Synchronous Chip Select |
| \overline{BWx} (x=a,b,c,d) | Synchronous Byte Write Controls |

| Symbol | Pin Name |
|------------------|---|
| \overline{BWE} | Byte Write Enable |
| \overline{OE} | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| NC | No Connect |
| DQx | Data Inputs/Outputs |
| DQPx | Data Inputs/Outputs |
| VDD | 3.3V/2.5V Power Supply |
| VDDQ | Isolated Output Power Supply 3.3V/2.5V |
| Vss | Ground |

165 PBGA PACKAGE PIN CONFIGURATION
 2M x 18 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|----------|------------------|-----------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-----------------|------------------|
| A | NC | A | \overline{CE} | \overline{BWb} | NC | $\overline{CE2}$ | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A | A |
| B | NC | A | CE2 | NC | \overline{BWA} | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A | NC |
| C | NC | NC | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | DQP _a |
| D | NC | DQ _b | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| E | NC | DQ _b | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| F | NC | DQ _b | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| G | NC | DQ _b | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | NC | DQ _a |
| H | NC | NC | NC | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | NC | NC | ZZ |
| J | DQ _b | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| K | DQ _b | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| L | DQ _b | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| M | DQ _b | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQ _a | NC |
| N | DQP _b | NC | V _{DDQ} | V _{SS} | NC | A | NC | V _{SS} | V _{DDQ} | NC | NC |
| P | NC | NC | A | A | NC | A1* | NC | A | A | A | A |
| R | MODE | A | A | A | NC | A0* | NC | A | A | A | A |

Note: * A₀ and A₁ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

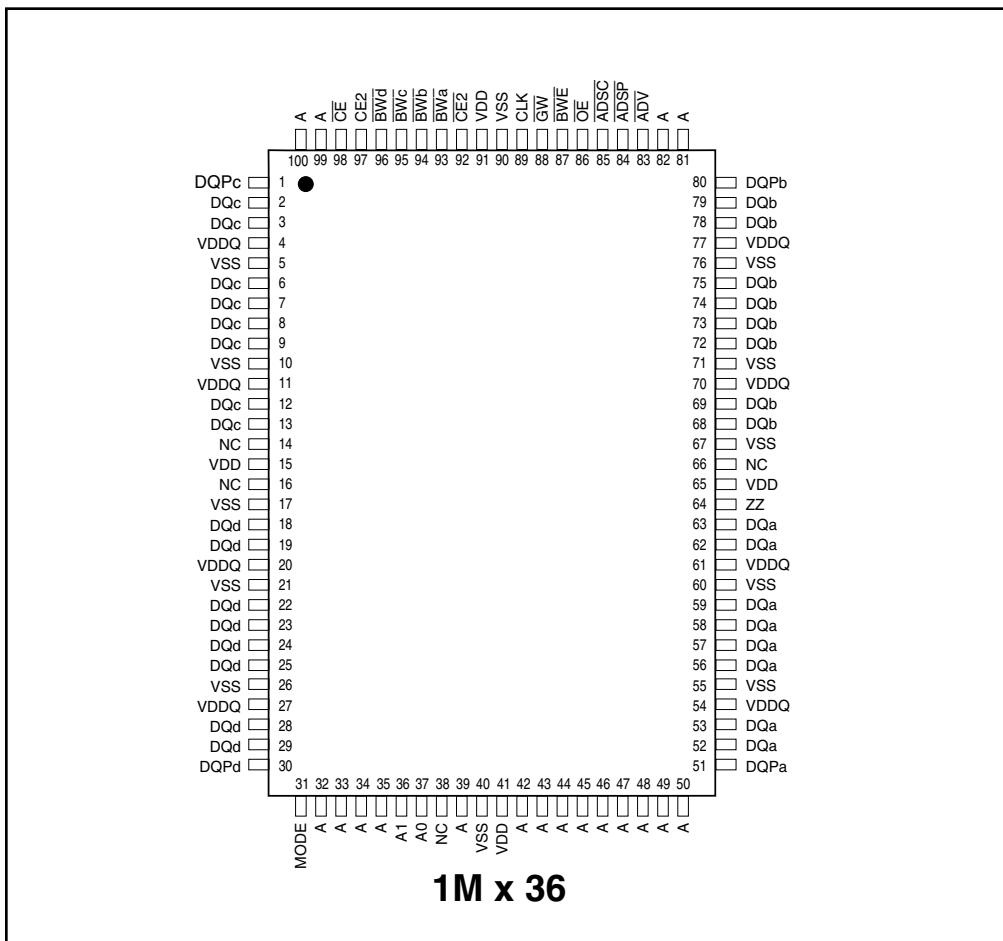
PIN DESCRIPTIONS

| Symbol | Pin Name |
|--|-----------------------------------|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| \overline{ADV} | Synchronous Burst Address Advance |
| \overline{ADSP} | Address Status Processor |
| \overline{ADSC} | Address Status Controller |
| \overline{GW} | Global Write Enable |
| CLK | Synchronous Clock |
| \overline{CE} , $\overline{CE2}$, CE2 | Synchronous Chip Select |
| \overline{BWx} (x=a,b) | Synchronous Byte Write Controls |

| Symbol | Pin Name |
|------------------|---|
| \overline{BWE} | Byte Write Enable |
| \overline{OE} | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| NC | No Connect |
| DQ _x | Data Inputs/Outputs |
| DQP _x | Data Inputs/Outputs |
| V _{DD} | 3.3V/2.5V Power Supply |
| V _{DDQ} | Isolated Output Power Supply 3.3V/2.5V |
| V _{SS} | Ground |

PIN CONFIGURATION

100-PIN TQFP



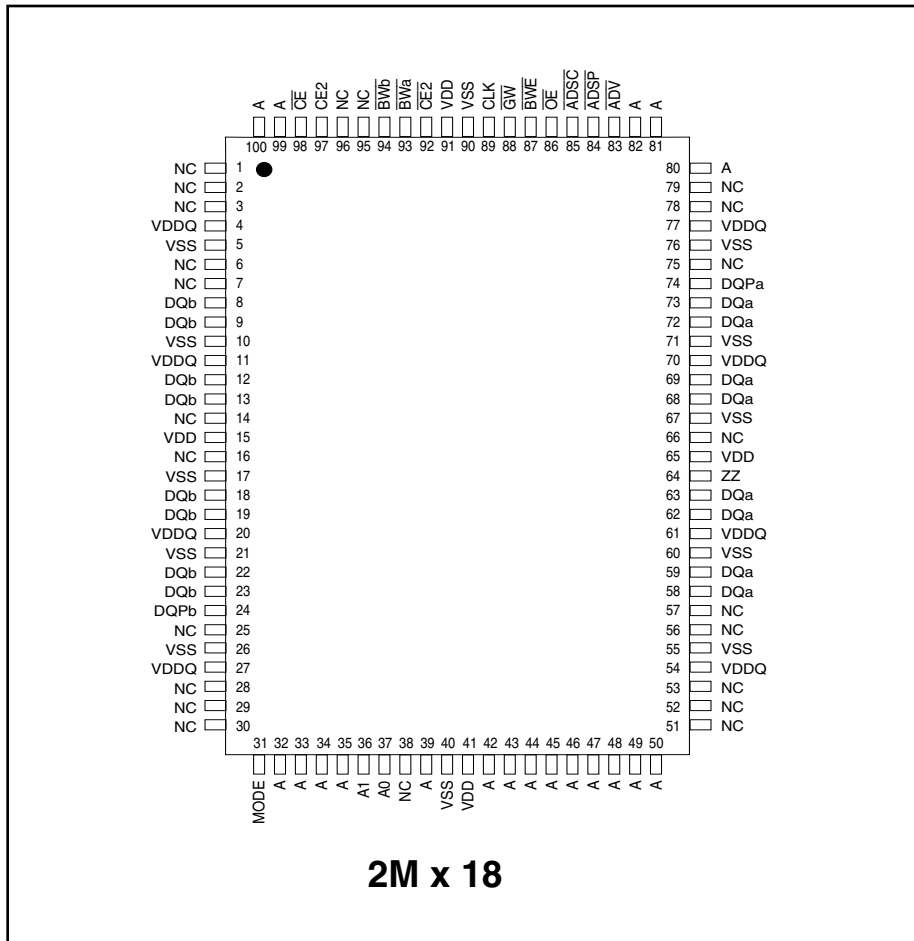
PIN DESCRIPTIONS

| | |
|--------------|--|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A | Synchronous Address Inputs |
| ADSC | Synchronous Controller Address Status |
| ADSP | Synchronous Processor Address Status |
| ADV | Synchronous Burst Address Advance |
| BWA-BWd | Synchronous Byte Write Enable |
| BWE | Synchronous Byte Write Enable |
| CE, CE2, CE2 | Synchronous Chip Enable |
| CLK | Synchronous Clock |

| | |
|-----------|---|
| DQa-DQd | Synchronous Data Input/Output |
| DQPd-DQPd | Parity Data Input/Output |
| GW | Synchronous Global Write Enable |
| MODE | Burst Sequence Mode Selection |
| OE | Output Enable |
| VDD | 3.3V/2.5V Power Supply |
| VDDQ | Isolated Output Buffer Supply: 3.3V/2.5V |
| VSS | Ground |
| ZZ | Snooze Enable |

PIN CONFIGURATION

100-PIN TQFP



PIN DESCRIPTIONS

| | | | |
|---|---|-----------------|---|
| A0, A1 | Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus. | DQPa-DQPb | Parity Data I/O; DQPa is parity for DQa1-8; DQPb is parity for DQb1-8 |
| A | Synchronous Address Inputs | \overline{GW} | Synchronous Global Write Enable |
| \overline{ADSC} | Synchronous Controller Address Status | MODE | Burst Sequence Mode Selection |
| \overline{ADSP} | Synchronous Processor Address Status | \overline{OE} | Output Enable |
| \overline{ADV} | Synchronous Burst Address Advance | VDD | 3.3V/2.5V Power Supply |
| $\overline{BWA-BWb}$ | Synchronous Byte Write Enable | VDDQ | Isolated Output Buffer Supply: 3.3V/2.5V |
| \overline{BWE} | Synchronous Byte Write Enable | VSS | Ground |
| $\overline{CE}, \overline{CE2}, \overline{CE2}$ | Synchronous Chip Enable | ZZ | Snooze Enable |
| CLK | Synchronous Clock | | |
| DQa-DQb | Synchronous Data Input/Output | | |

TRUTH TABLE⁽¹⁻⁸⁾ (3CE option)

| OPERATION | ADDRESS | \overline{CE} | $\overline{CE2}$ | CE2 | ZZ | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | \overline{WRITE} | \overline{OE} | CLK | DQ |
|-----------------------------|----------|-----------------|------------------|-----|----|-------------------|-------------------|------------------|--------------------|-----------------|-----|--------|
| Deselect Cycle, Power-Down | None | H | X | X | L | X | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | H | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | H | L | X | X | X | L-H | High-Z |
| Snooze Mode, Power-Down | None | X | X | X | H | X | X | X | X | X | X | High-Z |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | H | L-H | High-Z |
| Write Cycle, Begin Burst | External | L | L | H | L | H | L | X | L | X | L-H | D |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L-H | High-Z |
| Write Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| Write Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L-H | High-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L-H | High-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| Write Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For \overline{WRITE} , L means one or more byte write enable signals ($\overline{BWA-h}$) and \overline{BWE} are LOW or \overline{GW} is LOW. $\overline{WRITE} = H$ for all \overline{BWx} , \overline{BWE} , \overline{GW} HIGH.
3. \overline{BWA} enables WRITES to DQa's and DQPa. \overline{BWB} enables WRITES to DQb's and DQPb. \overline{BWC} enables WRITES to DQc's and DQPc. \overline{BWD} enables WRITES to DQd's and DQPd. DQPa-DQPd are available on the x36 version.
4. All inputs except \overline{OE} and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, \overline{OE} must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. \overline{ADSP} LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and \overline{BWE} LOW or \overline{GW} LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

TRUTH TABLE⁽¹⁻⁸⁾ (1CE option)

| NEXT CYCLE | ADDRESS | \overline{OE} | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | WRITE | \overline{OE} | DQ |
|-----------------------|----------|-----------------|-------------------|-------------------|------------------|-------|-----------------|--------|
| Deselected | None | H | X | L | X | X | X | High-Z |
| Read, Begin Burst | External | L | L | X | X | X | L | Q |
| Read, Begin Burst | External | L | L | X | X | X | H | High-Z |
| Write, Begin Burst | External | L | H | L | X | L | X | D |
| Read, Begin Burst | External | L | H | L | X | H | L | Q |
| Read, Begin Burst | External | L | H | L | X | H | H | High-Z |
| Read, Continue Burst | Next | X | H | H | L | H | L | Q |
| Read, Continue Burst | Next | X | H | H | L | H | H | High-Z |
| Read, Continue Burst | Next | H | X | H | L | H | L | Q |
| Read, Continue Burst | Next | H | X | H | L | H | H | High-Z |
| Write, Continue Burst | Next | X | H | H | L | L | X | D |
| Write, Continue Burst | Next | H | X | H | L | L | X | D |
| Read, Suspend Burst | Current | X | H | H | H | H | L | Q |
| Read, Suspend Burst | Current | X | H | H | H | H | H | High-Z |
| Read, Suspend Burst | Current | H | X | H | H | H | L | Q |
| Read, Suspend Burst | Current | H | X | H | H | H | H | High-Z |
| Write, Suspend Burst | Current | X | H | H | H | L | X | D |
| Write, Suspend Burst | Current | H | X | H | H | L | X | D |

NOTE:

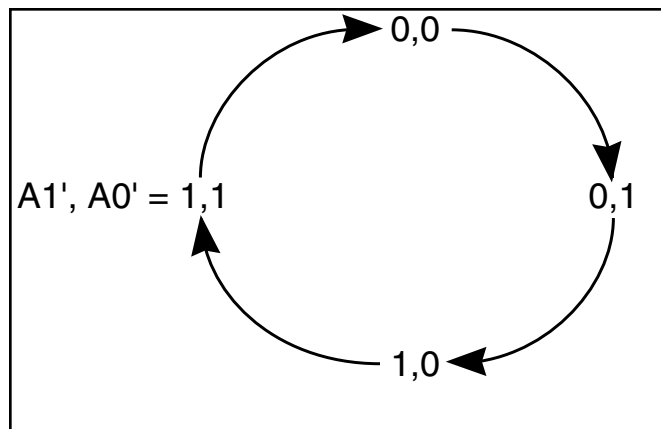
1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For WRITE, L means one or more byte write enable signals ($\overline{BWA-h}$) and \overline{BWE} are LOW or \overline{GW} is LOW. WRITE = H for all \overline{BWx} , BWE, GW HIGH.
3. \overline{BWA} enables WRITES to DQa's and DQPa. \overline{BWB} enables WRITES to DQb's and DQPb. \overline{BWC} enables WRITES to DQc's and DQPc. \overline{BWD} enables WRITES to DQd's and DQPd. DQPa-DQPd are available on the x36 version.
4. All inputs except OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, \overline{OE} must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. \overline{ADSP} LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE LOW or GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE

| Function | \overline{GW} | \overline{BWE} | \overline{BWA} | \overline{BWB} | \overline{BWC} | \overline{BWD} |
|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write Byte 1 | H | L | L | H | H | H |
| Write All Bytes | H | L | L | L | L | L |
| Write All Bytes | L | X | X | X | X | X |

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---------------------------|----------------------------|----------------------------|----------------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|------------------------------------|---|--------------------------------|------|
| T _{STG} | Storage Temperature | -55 to +150 | °C |
| P _D | Power Dissipation | 1.6 | W |
| I _{OUT} | Output Current (per I/O) | 100 | mA |
| V _{IN} , V _{OUT} | Voltage Relative to V _{SS} for I/O Pins | -0.5 to V _{DDQ} + 0.5 | V |
| V _{IN} | Voltage Relative to V _{SS} for for Address and Control Inputs | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | Voltage on V _{DD} Supply Relative to V _{SS} | -0.5 to 4.6 | V |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61LPSXXXXX)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

OPERATING RANGE (IS61VPSXXXXX)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | -40°C to +85°C | 2.5V ± 5% | 2.5V ± 5% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | 3.3V | | 2.5V | | Unit |
|-----------------|------------------------|---|------|-----------------------|------|-----------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -4.0 mA (3.3V) I _{OH} = -1.0 mA (2.5V) | 2.4 | — | 2.0 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V) | — | 0.4 | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | 1.7 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.7 | V |
| I _{LI} | Input Leakage Current | V _{SS} ≤ V _{IN} ≤ V _{DD} ⁽¹⁾ | -5 | 5 | -5 | 5 | μA |
| I _{LO} | Output Leakage Current | V _{SS} ≤ V _{OUT} ≤ V _{DDQ} , OE = V _{IH} | -5 | 5 | -5 | 5 | μA |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | Temp. range | -200 MAX | | -166 MAX | | Unit |
|------------------|--------------------------------|--|-------------------------------------|-------------------|------------|-------------------|------------|------|
| | | | | x18 | x36 | x18 | x36 | |
| I _{CC} | AC Operating Supply Current | Device Selected, OE = V _{IH} , ZZ ≤ V _{IL} , All Inputs ≤ 0.2V or ≥ V _{DD} - 0.2V, Cycle Time ≥ t _{kc} min. | Com. Ind. typ. ⁽²⁾ | 450 475 390 | 450 475 | 400 450 340 | 400 450 | mA |
| I _{SB} | Standby Current TTL Input | Device Deselected, V _{DD} = Max., All Inputs ≤ V _{IL} or ≥ V _{IH} , ZZ ≤ V _{IL} , f = Max. | Com. Ind. | 150 160 | 150 160 | 140 150 | 140 150 | mA |
| I _{SBI} | Standby Current CMOS Input | Device Deselected, V _{DD} = Max., V _{IN} ≤ V _{SS} + 0.2V or ≥ V _{DD} - 0.2V f = 0 | Com. Ind. typ. ⁽²⁾ | 110 140 75 | 110 140 | 110 140 75 | 110 140 | mA |

Note:

- MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100μA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} - 0.2V.
- Typical values are measured at V_{CC} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

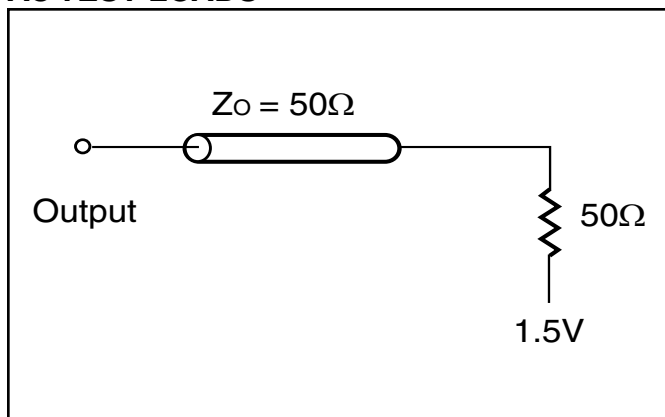


Figure 1

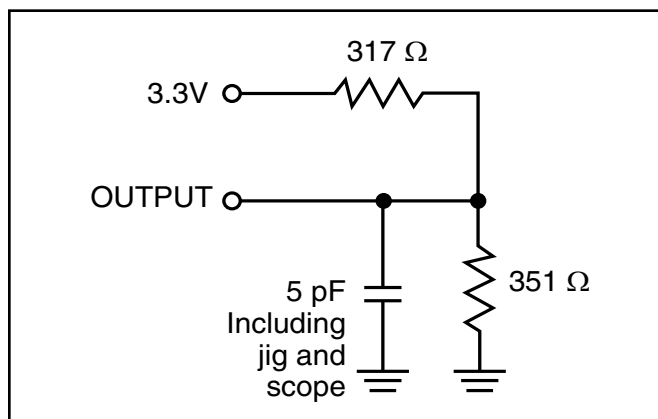


Figure 2

2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| Output Load | See Figures 3 and 4 |

2.5 I/O OUTPUT LOAD EQUIVALENT

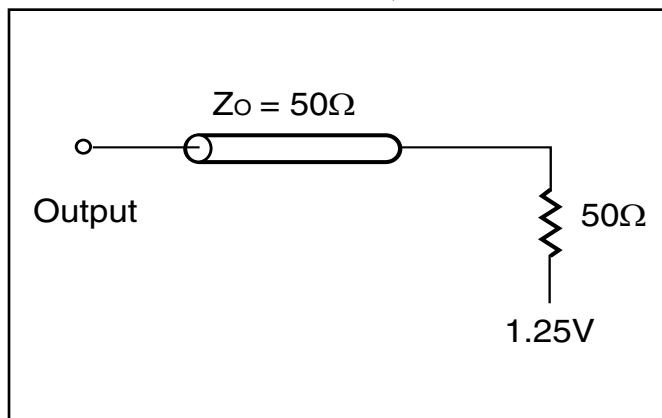


Figure 3

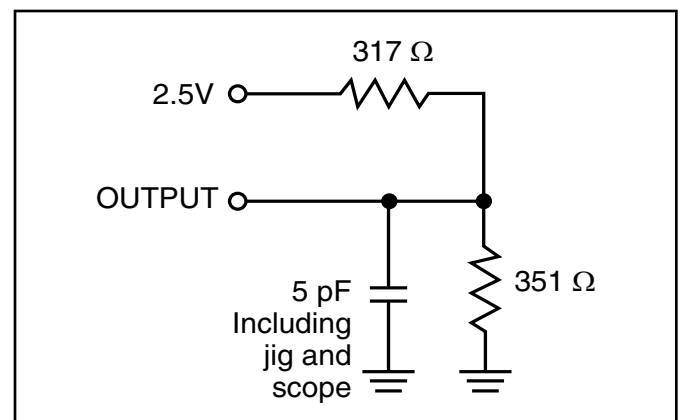


Figure 4

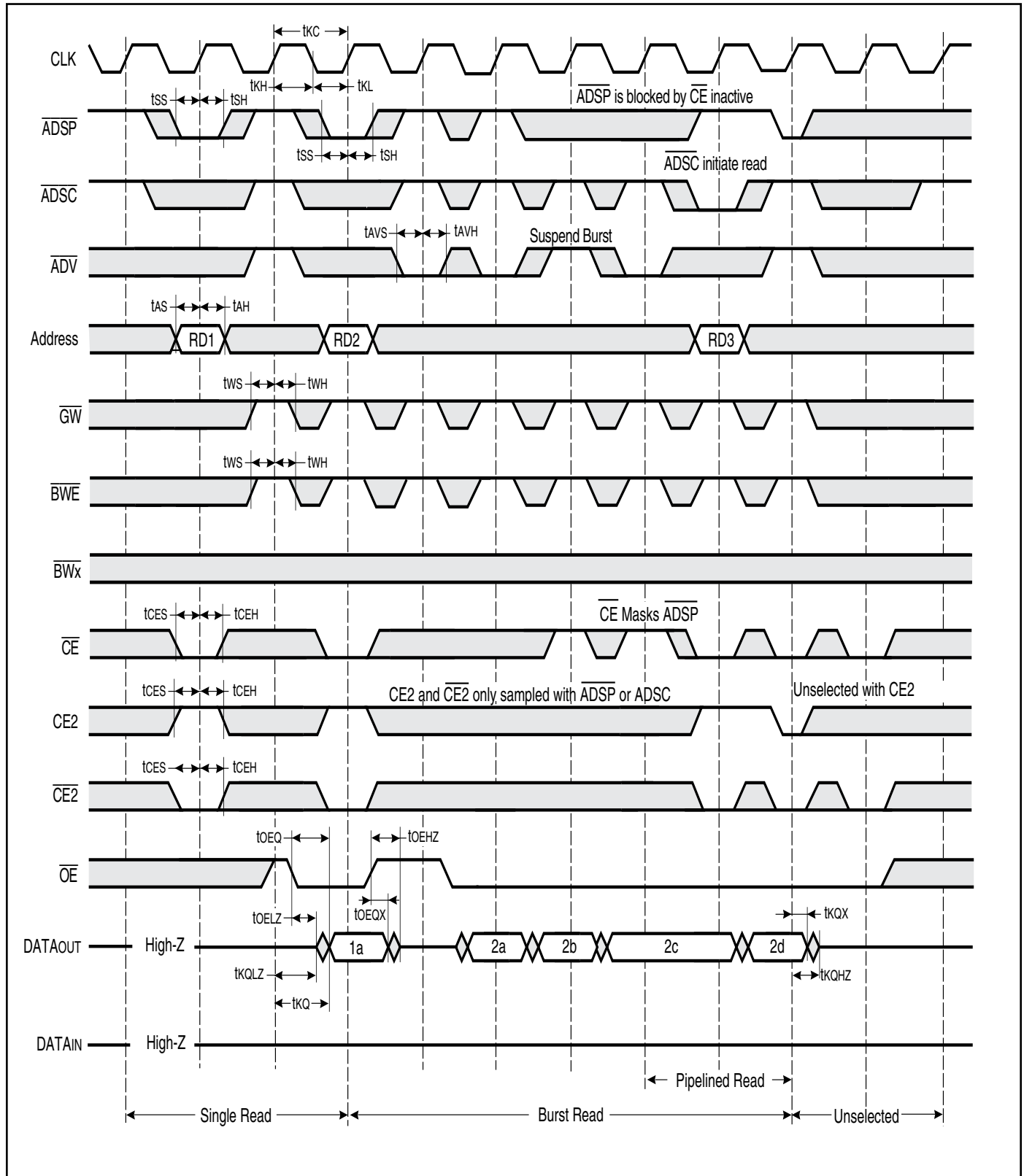
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | -200 | | -166 | | Unit |
|------------------------------------|----------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| f _{MAX} | Clock Frequency | — | 200 | — | 166 | MHz |
| t _{KC} | Cycle Time | 5 | — | 6 | — | ns |
| t _{KH} | Clock High Time | 2 | — | 2.4 | — | ns |
| t _{KL} | Clock Low Time | 2 | — | 2.4 | — | ns |
| t _{KQ} | Clock Access Time | — | 3.1 | — | 3.5 | ns |
| t _{KQX} ⁽²⁾ | Clock High to Output Invalid | 1.5 | — | 1.5 | — | ns |
| t _{KQLZ} ^(2,3) | Clock High to Output Low-Z | 1 | — | 1 | — | ns |
| t _{KQHZ} ^(2,3) | Clock High to Output High-Z | — | 3.0 | — | 3.4 | ns |
| t _{OEQ} | Output Enable to Output Valid | — | 3.1 | — | 3.5 | ns |
| t _{OEQX} ⁽²⁾ | Output Disable to Output Invalid | 0 | — | 0 | — | ns |
| t _{OELZ} ^(2,3) | Output Enable to Output Low-Z | 0 | — | 0 | — | ns |
| t _{OEHZ} ^(2,3) | Output Disable to Output High-Z | — | 3.0 | — | 3.4 | ns |
| t _{AS} | Address Setup Time | 1.4 | — | 1.5 | — | ns |
| t _{SS} | Address Status Setup Time | 1.4 | — | 1.5 | — | ns |
| t _{WS} | Read/Write Setup Time | 1.4 | — | 1.5 | — | ns |
| t _{CES} | Chip Enable Setup Time | 1.4 | — | 1.5 | — | ns |
| t _{AVS} | Address Advance Setup Time | 1.4 | — | 1.5 | — | ns |
| t _{DS} | Data Setup Time | 1.4 | — | 1.5 | — | ns |
| t _{AH} | Address Hold Time | 0.4 | — | 0.5 | — | ns |
| t _{SH} | Address Status Hold Time | 0.4 | — | 0.3 | — | ns |
| t _{WH} | Write Hold Time | 0.4 | — | 0.5 | — | ns |
| t _{CEH} | Chip Enable Hold Time | 0.4 | — | 0.5 | — | ns |
| t _{AVH} | Address Advance Hold Time | 0.4 | — | 0.5 | — | ns |
| t _{DH} | Data Hold Time | 0.4 | — | 0.5 | — | ns |
| t _{PDS} | ZZ High to Power Down | — | 2 | — | 2 | cyc |
| t _{PUS} | ZZ Low to Power Down | — | 2 | — | 2 | cyc |

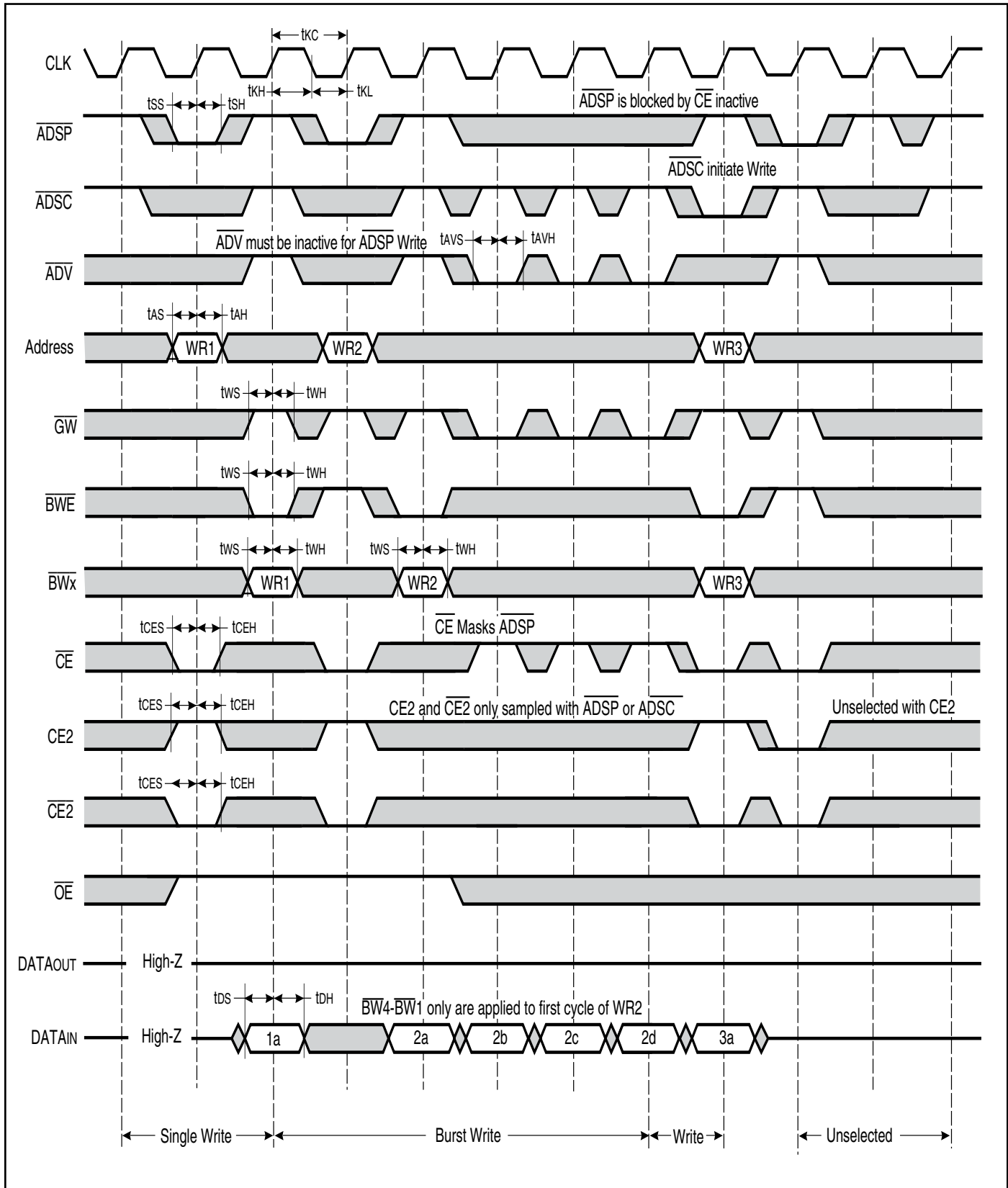
Note:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING



WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Temperature | Conditions | Min. | Max. | Unit |
|------------|------------------------------------|--------------|------------------|--------|----------|-------|
| ISB2 | Current during SNOOZE MODE | Com. Ind. | $ZZ \geq V_{ih}$ | — — | 60 90 | mA |
| t_{PDS} | ZZ active to input ignored | | | — | 2 | cycle |
| t_{PUS} | ZZ inactive to input sampled | | | 2 | — | cycle |
| t_{ZZI} | ZZ active to SNOOZE current | | | — | 2 | cycle |
| t_{RZZI} | ZZ inactive to exit SNOOZE current | | | 0 | — | ns |

SNOOZE MODE TIMING



**ORDERING INFORMATION (3.3V core/2.5V-3.3V I/O)****Commercial Range: 0°C to +70°C**

| Configuration | Frequency | Order Part Number | Package |
|---------------|-----------|-----------------------|---------------------|
| 1Mx36 | 166 | IS61LPS102436A-166TQ | 100 TQFP |
| | | IS61LPS102436A-166TQL | 100 TQFP, Lead-free |
| | | IS61LPS102436A-166B3 | 165 PBGA |
| 2Mx18 | 166 | IS61LPS204818A-166TQ | 100 TQFP |
| | | IS61LPS204818A-166TQL | 100 TQFP, Lead-free |
| | | IS61LPS204818A-166B3 | 165 PBGA |

Industrial Range: -40°C to +85°C

| Configuration | Frequency | Order Part Number | Package |
|---------------|-----------|------------------------|---------------------|
| 1Mx36 | 166 | IS61LPS102436A-166TQI | 100 TQFP |
| | | IS61LPS102436A-166TQLI | 100 TQFP, Lead-free |
| | | IS61LPS102436A-166B3I | 165 PBGA |
| | | IS61LPS102436A-166B3LI | 165 PBGA, Lead-free |
| 2Mx18 | 166 | IS61LPS204818A-166TQI | 100 TQFP |
| | | IS61LPS204818A-166B3I | 165 PBGA |



IS61VPS102436A, IS61LPS102436A, IS61VPS204818A, IS61LPS204818A

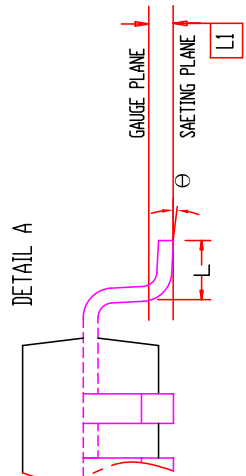
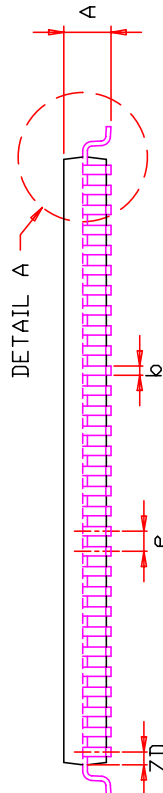
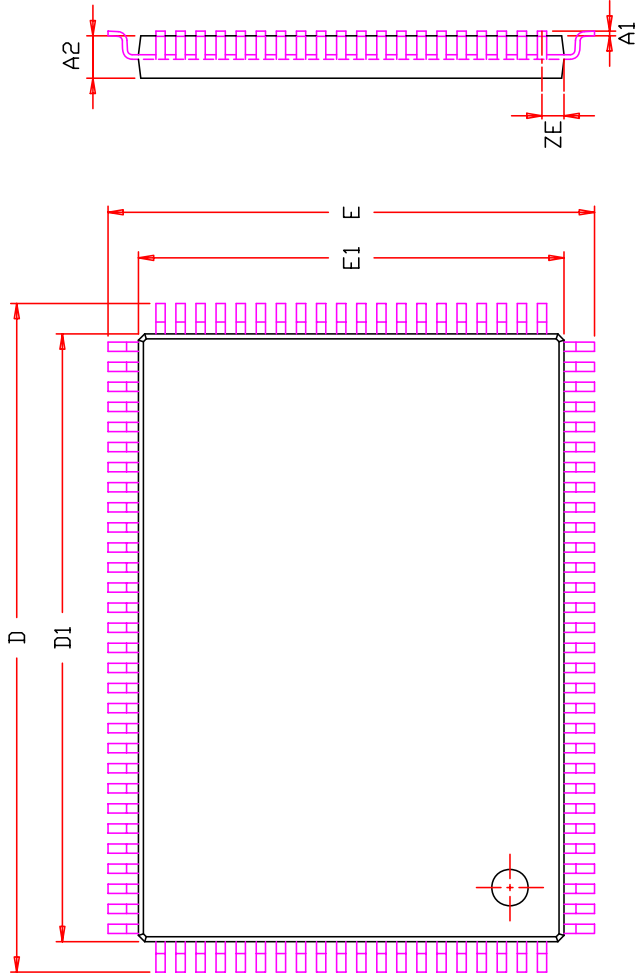
ORDERING INFORMATION (2.5V core/2.5V I/O)

Commercial Range: 0°C to +70°C

| Configuration | Frequency | Order Part Number | Package |
|---------------|-----------|-----------------------|---------------------|
| 1Mx36 | 166 | IS61VPS102436A-166TQ | 100 TQFP |
| | | IS61VPS102436A-166TQL | 100 TQFP, Lead-free |
| | | IS61VPS102436A-166B3 | 165 PBGA |
| 2Mx18 | 166 | IS61VPS204818A-166TQ | 100 TQFP |
| | | IS61VPS204818A-166TQL | 100 TQFP, Lead-free |
| | | IS61VPS204818A-166B3 | 165 PBGA |

Industrial Range: -40°C to +85°C

| Configuration | Frequency | Order Part Number | Package |
|---------------|-----------|-----------------------|----------|
| 2Mx18 | 166 | IS61VPS204818A-166TQI | 100 TQFP |
| | | IS61VPS204818A-166B3I | 165 PBGA |



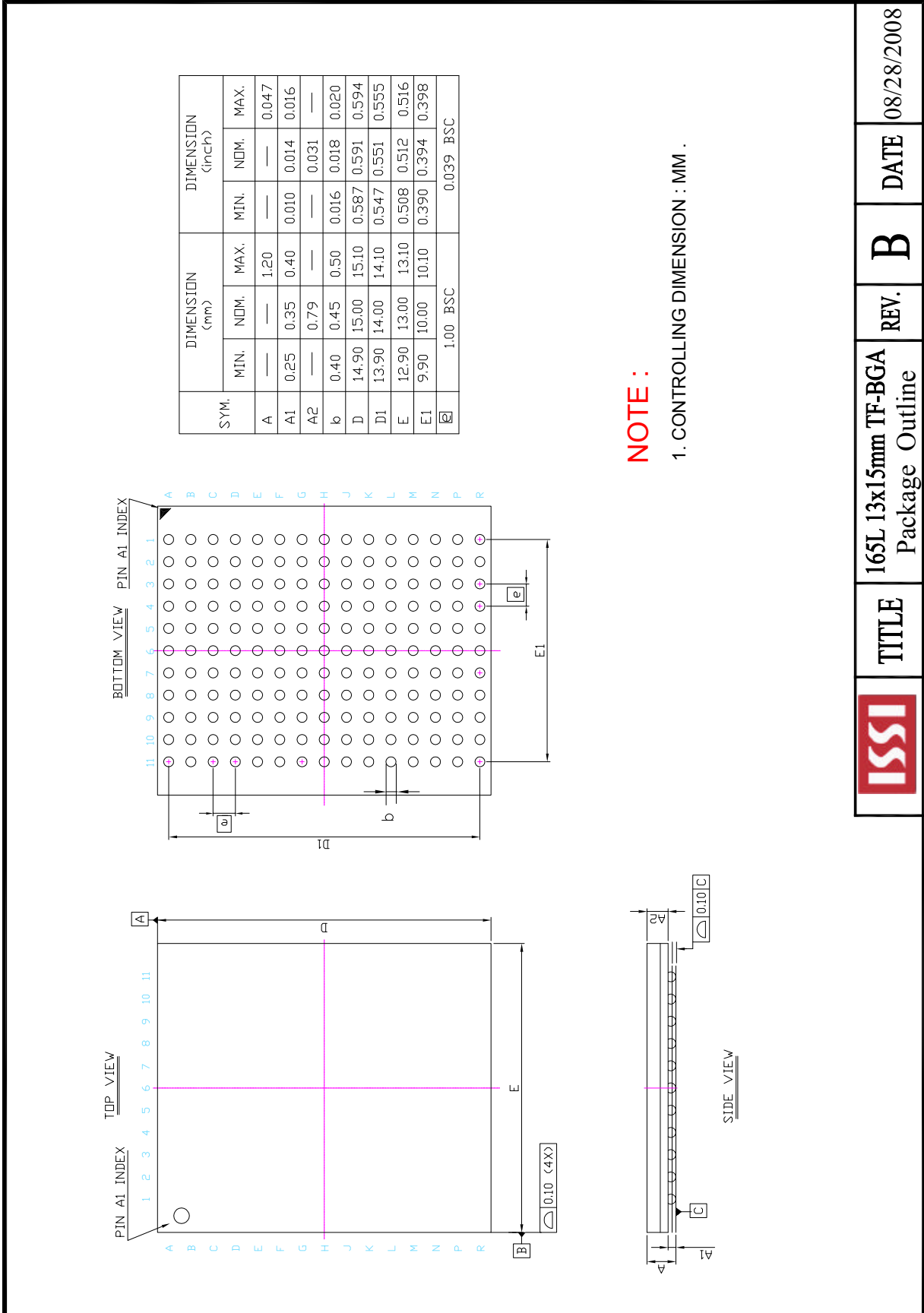
| SYMBOL | DIMENSION IN MM | | DIMENSION IN INCH | |
|--------|-----------------|-----------|-------------------|-----------|
| | MIN. | NDM. MAX. | MIN. | NDM. MAX. |
| A | 1.40 | 1.60 | 0.055 | 0.063 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 1.35 | 1.45 | 0.053 | 0.057 |
| b | 0.22 | 0.30 | 0.009 | 0.012 |
| D | 21.90 | 22.10 | 0.862 | 0.870 |
| D1 | 19.90 | 20.10 | 0.783 | 0.791 |
| E | 15.90 | 16.10 | 0.626 | 0.634 |
| E1 | 13.90 | 14.10 | 0.547 | 0.555 |
| e | 0.65 BSC. | | 0.026 BSC. | |
| L | 0.45 | 0.60 | 0.018 | 0.024 |
| L1 | 0.25 BSC. | | 0.010 BSC. | |
| ZD | 0.575 REF. | | 0.023 REF. | |
| ZE | 0.825 REF. | | 0.032 REF. | |
| theta | 0 | 3.5° | 0 | 3.5° |

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

| | | | |
|---|---|------|------------|
|  | TITLE | REV. | DATE |
| | 100L14x20x1.4mm LQFP (Footprint : 2.0 mm) Package Outline | F | 09/01/2009 |

280-600-011 REV. A



NOTE :

1. CONTROLLING DIMENSION : MM .



TITLE

**165L 13x15mm TF-BGA
Package Outline**

B

REV.

DATE 08/28/2008